Secure Digital Card

Table of Contents

Revision History

Revision	Date	History	Remark
A.0	01/04 '07	New Creation	

1. Introduction to the SD Card

The SD Card is a memory card that is small and thin with SDMI. SD Card is a Flash–Based memory card that is designed to meet the security, capacity, performance and environment requirements inherent to use in emerging audio and video electronic device.
The SD Card includes a copyright protection mechanism that complies with the security of the SDMI standard (SDMI: Secure Digital Music Initiative).
The SD Card communication is based on an advance 9-pin interface (clock, command, 4x Data and 3x power lines) and the SD Card host interface supports regular MultiMediaCard operation as well.

2. SD Card Feature

- Flash memory card capacity support list below:
  Standard Capacity SD Memory Card:
  - 256MB
  - 512MB
  - 1GB
  - 2GB

  High Capacity SD Memory Card:
  - 4GB
  - 8GB
  - 16GB
  - 32GB

- Compliant SDA Specification ver 2.0
- Variable clock rate:
  - Default mode: 0-25 MHz, up to 12.5MB/sec interface speed.
  - High-speed mode:0-50 MHz, up to 25MB/sec interface speed.

- High Capacity SD Memory Cards shall support Speed Class Specification and have performance more Than or equal to Class 2, it includes:
  - Class 2
  - Class 4
  - Class 6

- Support CPRM
- No external programming voltage required
- SD Card protocol compatible
- Targeted for portable and stationary applications for secured (copyrights protected) and non-secured data storage
- Correction of memory field errors
- Copyrights Protection Mechanism: Complies with highest security of SDMI standard.
- Password Protection of cards (CMD42-LOCK_UNLOCK).
- Card detection command (Insertion / Removal)
- CE and FCC certificates
- Easy handling for the end user

Notes: The performance depends on different test platform with different result.
・The communication channel is described in the table

SD Bus/SPI Bus comparison

SD Card Using SD Bus	SD Card Using SPI Bus
Six-wire communication channel (clock, command, 4 data lines)	Three-wire serial data bus (Clock, dataIn, dataOut)+card specific CS signal(hardwired card selection)
Error-protected data transfer	Optional non protected data transfer mode available
Single or multiple block oriented data transfer	Single or multiple block oriented data transfer

3. Product Specification

3.1 System Environment Specifications

Temperature	Operating: Non-Operating:	-25℃ to 85℃ -40℃ (168h) to 85℃(500h)
Moisture and corrosion	Operating: Non-Operating:	25°C / 95% rel. humidity 40°C / 93% rel. hum./500h salt water spray: 3% NaCl/35C; 24h acc. MIL STD Method 1009
Vibration	Operating: Non-Operating:	15 G peak to peak max. 15 G peak to peak max.
Shock	Operating: Non-Operating:	1,000 G max. 1,000 G max.
Altitude (relative to sea level)	Operating: Non-Operating:	80,000 feet max. 80,000 feet max.

3.2 Reliability and Durability Specifications

Durability	10,000 mating cycles
Bending	10N
Torque	0.15N.m or +/-2.5 deg.
Drop Test	1.5m free fall
UV Light Exposure	UV: 254nm, 15Ws/cm^2 according to IOS 7816-1
X-ray exposure	0.1 Gy of medium-energy radiation (70 keV to 140 keV, cumulative dose per year) to both sides of the card, according to ISO7816-1.
Visual Inspection/Shape and Form	No warp age; no mold slim; complete form; no cavities; surface smoothness≦-0.1 mm/cm^2 within contour; no cracks; no pollution (oil, dust, etc.)

3.3 Typical Card Pow Requirement

VDD (fipple: max,60mV peak to peak)	2.7V~3.6V

3.4 System Reliability and Maintenance

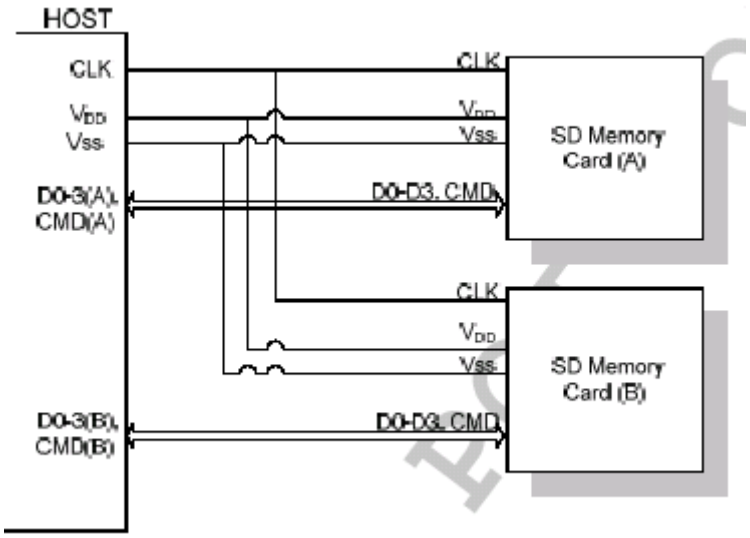
MTBF	>1,000,000 hours
Preventive Maintenance	None
Data Reliability	< 1 non-recoverable error in 10^{14} bits read
Endurance	100,000 write/erase cycles (SLC NAND flash) 10,000 write/erase cycles (MLC NAND flash)

3.5 SD Bus Topology

The SD bus has six communication lines and two supply lines:

- CMD: Command is bi-directional signal. (Host and card drivers are operating in push pull mode.)
- DAT0-3: Data lines are bi-directional signals. (Host and card drivers are operating in push pull mode.)
- CLK: Clock is a host to cards signal. (CLK operates in push pull mode.)
- VDD: VDD is the power supply line for all cards
- VSS: VSS are two ground lines

The following figure shows the bus topology of several cards with one host in SD Bus mode.



SD Memory Card System Bus Topology

During the initialization process, commands are sent to each card individually, allowing the application to detect the cards and assign logical addresses to the physical slots. Data is always sent to each card individually. However, to simplify the handling of the card stack, after initialization, all commands may be sent concurrently to all cards. Addressing information is provided in the command packet.

The SD Bus allows dynamic configuration of the number of data lines. After power-up, by default, the SD Card will use only DAT0 for data transfer. After initialization, the host can change the bus width (number of active data lines). This feature allows and easy trade off between hardware cost and system performance.

3.6 SPI Bus Topology

The SD Card SPI interface is compatible with SPI hosts available on the market. As any other SPI device the SD Card SPI channel consists of the following 4 signals:

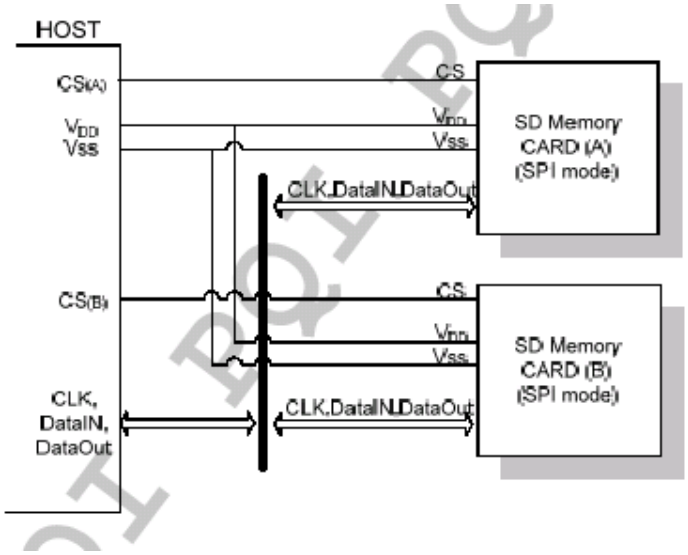
1) CS: Host to card Chip Select signal.
2) SCLK: Host to card clock signal.
3) DataIn: Host to card data signal.
4) DataOut: Card to host data signal.

Another SPI common characteristic, which is implemented in the SD Card as well, is byte transfers. All data tokens are multiples of 8 bit bytes and always byte aligned to the CS signal.

The SPI standard defines the physical link only and not the complete data transfer protocol. In SPI Bus mode, the SD Card uses a subset of the SD Card protocol and command set.

The SD Card identification and addressing algorithms are replaced by a hardware Chip Select (CS) signal. A card (slave) is selected, for every command, by asserting (active low) the CS signal.

The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception is card programming time. At this time the host can de-assert the CS signal without affecting the programming process.



SD Memory Card System (SPI Mode) Bus Topology

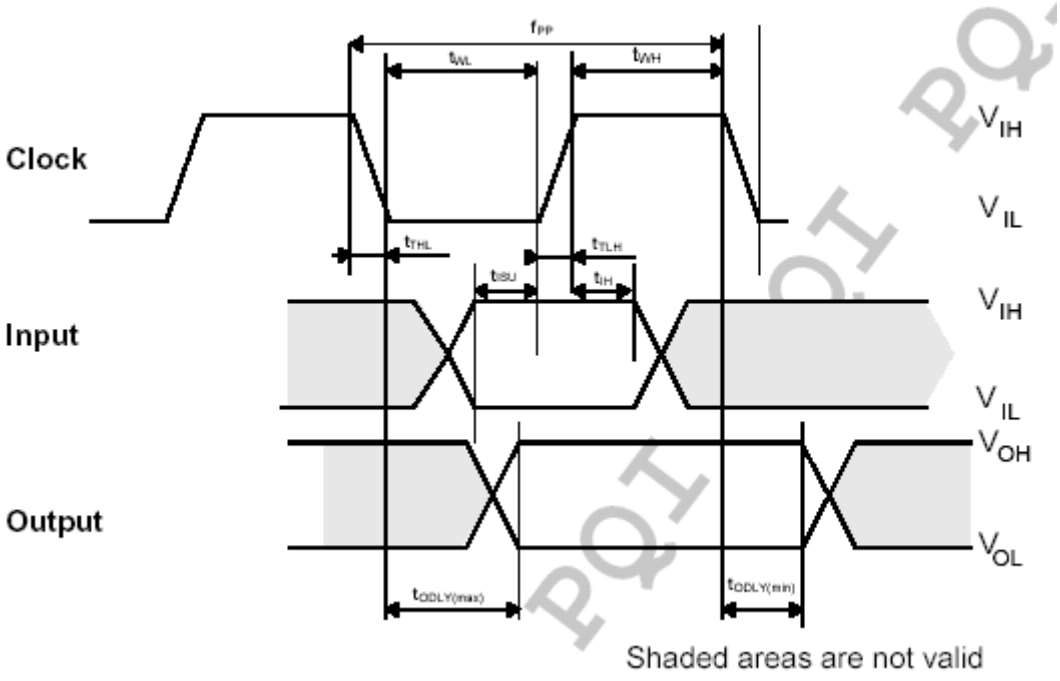
3.7 Electrical Interface

The power up of the SD Card bus is handled locally in each SD Card and in the bus master.
SPI Mode bus operating conditions are identical to SD Card mode bus operating conditions. The CS (chip select) signal timing is identical to the input signal timing.

Power Supply Voltage

General					
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**	**Remark**
Peak voltage on all lines		-0.3	VDD+ 0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	
Power supply Voltage					
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**	**Remark**
Supply Voltage for voltage range	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75* V_{DD}		V	I_{OH}=-100uA $V_{DD\ min}$
Output Low Voltage	V_{OL}		0.125* V_{DD}	V	I_{OL}=-100uA $V_{DD\ min}$
Input High Voltage	V_{IH}	0.625* V_{DD}	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	V_{DD}-0.3	0.25* V_{DD}	V	
Power up time			250	ms	From 0V to $V_{DD\ min}$

3.8 Bus Timing (Default)

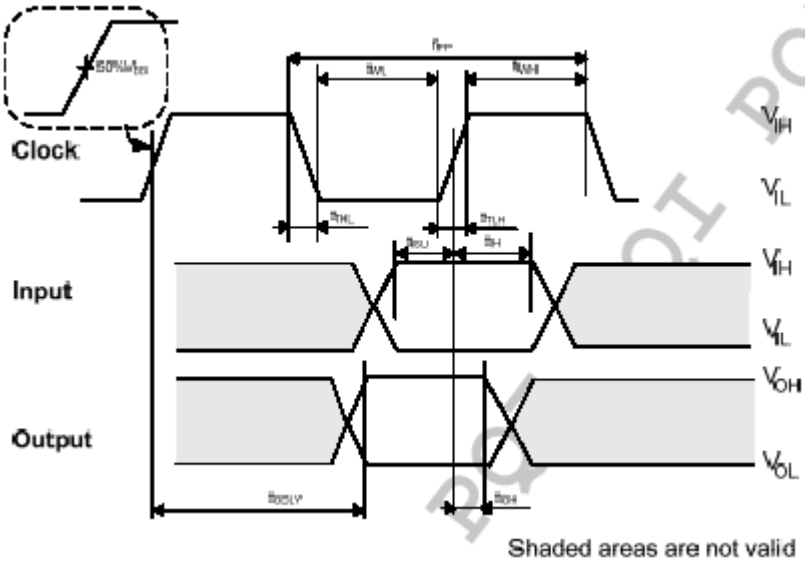


Timing Diagram Data Input/Output Referenced to Clock(Default)

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min.(VIH) and max.(VIL))					
Clock Frequency Data Transfer Mode	f_{PP}	0	25	MHz	$C_{CARD} \leqq$ 10 pF (1 card)
Clock Frequency Identification Mode	f_{OD}	0/100	400	KHz	$C_{CARD} \leqq$ 10 pF (1 card)
Clock Low Time	t_{WL}	10		ns	$C_{CARD} \leqq$ 10 pF (1 card)
Clock High Time	t_{WH}	10		ns	$C_{CARD} \leqq$ 10 pF (1 card)
Clock Rise Time	t_{TLH}		10	ns	$C_{CARD} \leqq$ 10 pF (1 card)
Clock Fall Time	t_{THL}		10	ns	$C_{CARD} \leqq$ 10 pF (1 card)
Inputs CMD,DAT(referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	$C_{CARD} \leqq$ 10 pF (1 card)
Input hold time	t_{IH}	5		ns	$C_{CARD} \leqq$ 10 pF (1 card)
Outputs CMD,DAT(referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	$C_L \leqq$ 40 Pf (1 card)
Output Delay time during Identification Mode	t_{ODLY}	0	50	ns	$C_L \leqq$ 40 pF (1 card)

Bus Timing-Parameters Values (Default)

3.9 Bus Timing (High-Speed Mode)



Timing Diagram Data Input/Output Referenced to Clock(High-Speed)

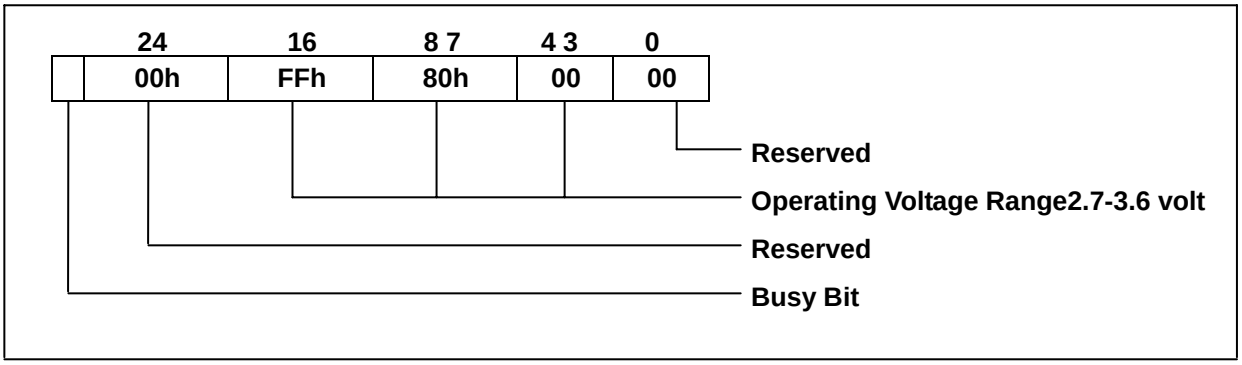
Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min.(VIH) and max.(VIL))					
Clock Frequency Data Transfer Mode	f_{PP}	0	50	MHz	$C_{CARD} \leqq$ 10 pF (1 card)
Clock Low Time	t_{WL}	7		ns	$C_{CARD} \leqq$ 10 pF (1 card)
Clock High Time	t_{WH}	7		ns	$C_{CARD} \leqq$ 10 pF (1 card)
Clock Rise Time	t_{TLH}		3	ns	$C_{CARD} \leqq$ 10 pF (1 card)
Clock Fall Time	t_{THL}		3	ns	$C_{CARD} \leqq$ 10 pF (1 card)
Inputs CMD,DAT(referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	$C_{CARD} \leqq$ 10 pF (1 card)
Input hold time	t_{IH}	2		ns	$C_{CARD} \leqq$ 10 pF (1 card)
Outputs CMD,DAT(referenced to CLK)					
Output Delay time during data Transfer Mode	t_{ODLY}	0	14	ns	$C_L \leqq$ 40 Pf (1 card)
Output Hold time	t_{OH}	2.5		ns	$C_L \geqq$ 15 pF (1 card)
Total System capacitance for each line	C_L		40	pF	1 card

Bus Timing-Parameters Values (High-Speed)

3.10 Operating Conditions Register (OCR)

The 32-bit operation conditions register stores the V_{DD} voltage profile of the card. The SD Card is capable of executing the voltage recognition procedure (CMD1) with any standard SD Card host using operating voltages form 2 to 3.6 Volts.

Accessing the data in the memory array, however, requires 2.7 to 3.6 Volts. The OCR shows the voltage range in which the card data can be accessed. The structure of the OCR register is described in under table.



OCR Structure

3.11 Card Identification (CID) Register

The CID register is 16 bytes long and contains a unique card identification number as shown in the table below. It is programmed during card manufacturing and can not be changed by SD Card hosts. Note that the CID register in the SD Card has a different structure than the CID register in the MultiMediaCard

Name	Field	Width	CID-Slice
Manufacturer ID	MID	8	[127:120]
OEM/Application ID	OID	16	[119:104]
Product name	PNM	40	[103:64]
Product version	PRV	8	[63:56]
Product serial number	PSN	32	[55:24]
Reserved	--	4	[23:20]
Manufacturing date	MDT	12	[19:8]
CRC7 checksum	CRC	7	[7:1]
Not use, always “1”	--	1	[0:0]

3.12 CSD Register

The Card Specific Data (CSD) register contains configuration information required in order to access the card data. In the table below, the cell type column defined the CSD field as Read only (R), One Time Programmable(R/W) or erasable(R/W/E). This table shows, for each field, the value in”real world” units and coded according to the CSD structure. The Model dependent column marks (with a check mark —√) the CSD fields which are model dependent. Note that the CSD register in the SD Card has a different structure than the CSD in the MultiMediaCard.

4. SD Card Interface Description

General Description of Pins and Registers

The SD Card has 9 exposed contacts on one side. The host is connected to the SD Card using a 9 pin connector.

Pin Assignment in SD Bus Mode Pad Definition

Pin #	Name	Type	SD Description
1	CD/DAT3	I/O	Card Detect / Data Line [Bit 3]
2	CMD	I/O	Command / Response
3	Vss1	S	Supply voltage ground
4	VDD	S	Supply voltage
5	CLK	I	Clock
6	Vss2	S	Supply voltage ground
7	DAT0	I/O	Data Line [Bit 0]
8	DAT1	I/O	Data Line [Bit 1]
9	DAT2	I/O	Data Line [Bit 2]

Note:

1. S=power supply; I=input; O=output using push-pull drivers.
2. The extended DAT lines (DAT1-DAT3) are input on power up; they start to operate as DAT lines after the SET_BUS_WIDTH command.
3. After power up, this line is input with 50Kohm pull-up (can be used for card detection or SPI mode selection). The pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command.

Pin Assignment in SPI Bus Mode Pad Definition

Pin #	Name	Type	SD Description
1	CS	I	Chip Select (active true)
2	DataIn	I	Host to card command and data
3	Vss1	S	Supply Voltage Ground
4	VDD	S	Supply Voltage
5	CLK	I	Clock
6	Vss2	S	Supply Voltage Ground
7	DataOut	O	Card to Host data and status
8	RSV	I	Reserved
9	RSV	I	Reserved

SD Card Registers

Name	Width	Description
CID	128	Card identification number: individual card number for identification.
RCA	16	Relative card address: local system address of a card, dynamically suggested by the card and approved by the host during initialization
DSR	16	Driver Stage Register; to configure the card's output drivers. Optional.
CSD	128	Card specific data: information about the card operation conditions.
SCR	64	SD Configuration Register: information about the microSD Card's special feature capabilities.
OCR	32	Operation Condition Register

The host may reset the cards by switching the power supply off and on again. The card has its own power-on detection circuitry which puts the card into an idle state after the power-on. The card can also be reset by sending the **GO_IDLE** (CMD0) command.

5. Physical Outline